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Please find below and/or attached an Office communication concerning this application or proceeding.

AY

Office Action Summary	Application No.	Applicant(s)
	09/517,345	ANDERSON ET AL.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 and 49-70 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 and 49-70 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03-24-04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The formal drawings filed on 01/02/1998 are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 20 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949) in view of Freyman et al. (US Pat. 5985695) and Kimura (US Pat. 5663594).

Regarding claim 20, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a metallized polymer layer (MPL)/flexible dielectric tape (FDT) substrate (59/60 in Fig. 3B/3A; Col. 7, lines 30-35) having a first/top side and a second/bottom side, the MPL/FDT defining a first thickness
- a transition medium/support structure (50 in Fig. 3B/3A) coupled to the MPL/FDT
- a silicon die (52 in Fig. 3B/3A) coupled to the transition medium

- a conventional plastic encapsulant/mold cap encapsulating the transition medium and the die (mold cap not numerically referenced- see Fig. 3B; Col. 8, line 40), the mold cap having a thickness comprising a thickness/second thickness above the transition medium, wherein the first and second thickness define a package thickness
- the die being disposed approximately in the middle of the package thickness measured from the bottom of the MPL/FDT to the top of the mold cap (see Fig. 3B), and
- solder balls (54 in Fig. 3A) and the die being electrically coupled to through respective bonding pads

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller fails to teach:

- a) dimensions of the die, transition medium and the package being such that the die is disposed near midline of the package and a first and a second edge of the transition medium being coincident with those of the die respectively, and
 - b) at least one solder ball and metallized polymer layer comprising a flat surface.
- a) The determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in chip packaging and encapsulation technology art is a subject of routine experimentation

and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

b) Kimura teaches a conventional BGA package having solder ball configuration such that the solder ball (106 in Fig. 1) and metallized resin/polymer substrate (111/113/114 in Fig. 1) comprise a flat surface (see 106 and 113/114 in Fig. 1) to provide an improved adhesion and bonding (Col. 1, lines 10-51).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the elements a) and b) as taught by Freyman et al. and Kimura so that the thermal dissipation, temperature variation within the package, and stress distribution can be optimized and the surface protection for the die and the bonding/reliability can be improved in Schueller's IC package.

Regarding claim 22, Schueller, Freyman et al. and Kimura teach substantially the entire claimed structure as applied to claim 20 above, wherein Schueller further teaches the silicon die being coupled/mounted to the transition medium through the adhesive (64 in Fig. 3B; Col. 9, line 65).

Regarding claim 23, Schueller, Freyman et al. and Kimura teach substantially the entire claimed structure as applied to claim 20 above, wherein Schueller further teaches the transition medium/support structure comprising a variety of material including PCB/FR-4 (Col. 10, lines 18-28), an adhesive, an elastomer, etc. (see 224 in Fig. 2 and 10 in Fig. 1; Col. 5, line 42; Col. 6, line 44; Col. 5 and 6).

Regarding claim 24, Schueller, Freyman et al. and Kimura teach substantially the entire claimed structure as applied to claim 20 above, wherein Schueller further teaches the metallized polymer layer being the tape carrier (59/60 in Fig. 3B/3A; Col. 7, lines 30-35).

4. Claims 1, 2, 4, 6-10, 12-16, 18, 19, 49-59 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949) in view of Zenner et al. (US Pat. 6246010) and Freyman et al. (US Pat. 5985695).

Regarding claim 1, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3B/3A) having a first thickness
- a metallized polymer layer/flexible dielectric tape substrate (59/60 in Fig. 3B/3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3B/3A) disposed between the silicon die and the first side of the metallized polymer layer where the transition medium/support structure has a second thickness

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller discloses using a single transition medium/support structure having a second thickness/layer of 100-250 microns (Col. 9, line 49) or using a plurality of those layers (Col. 11, line 12) but fails to teach:

a) the first thickness of the silicon die being less than the second thickness, and
b) a first and a second edge of the transition medium being coincident with those of the silicon die respectively.

a) Zenner et al. teach using a high density/thin package having a die thickness/first thickness where the die has been thinned/lapped to about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55; Col. 2-4) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

b) Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first thickness of the silicon die with a smaller thickness than the second thickness of transition medium as taught by Zenner et al. and

the first and a second edge of the transition medium being coincident with those of the silicon die respectively as taught by Freyman et al. so that the thermal stress can be reduced, the functionality/reliability can be improved and processing can be simplified in Schueller's IC package.

Regarding claims 2 and 6, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Schueller further teaches the transition medium/support structure comprising a single or multilayered structure including conventional conductive/non-conductive material such as ceramic, metal, PCB or a combination of metal and non-metal/epoxy PCB material (Col. 9, line 58; Col. 10, line 27; Col. 11, line 12). Furthermore, Schueller discloses selecting the transition medium/support structure to provide various functions such as improved strength (Col. 9, line 52), thermal dissipation (Col. 9, line 10), etc. so that the thermal stress and defects such as fracture, cracking, etc. can be reduced (Col. 6-10).

Regarding claim 4, Schueller, Zenner et al. and Freyman et al teach substantially the entire claimed structure as applied to claim 1 above, wherein Schueller further teaches the transition medium/support structure being made of conventional nonconductive epoxy/PCB/FR-4 type material (Col. 10, line 18-27).

Regarding claim 7, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Schueller further teaches the die being disposed approximately near the middle of a package having a thickness

where the package thickness is defined by the thickness of the metallized polymer layer/tape and that of the plastic encapsulant/mold cap (Col. 8, line 40; Fig. 3B), but fail to teach the die being disposed approximately equally spaced from the bottom of the metallized polymer layer and the top of the plastic encapsulant.

The determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the thickness of the encapsulant such that die is disposed approximately equally spaced from the bottom of the metallized polymer layer and the top of the plastic encapsulant so that the desired thermal/mechanical stress can be reduced and the and the reliability of the package can be improved in Freyman et al., Zenner et al. and Schueller's IC package.

Regarding claims 8 and 9, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claims 1, 5 and 7 above, except the thickness of the package and die being 0.06 inches/60 mils or less and 6 mils and less respectively.

Zenner et al. further teach using the high density/thin package having the die thickness of about less than 100 microns/4 mils and a package thickness of about 275 microns/11 mils (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the thickness of the package and the die to be less than approximately 0.060 inches and 6 mils respectively as taught by Zenner et al. so that the desired thermal/mechanical stress can be reduced and the reliability of the package can be improved in Freyman et al., Zenner et al. Schueller's IC package.

Regarding claim 10, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1, above, wherein Schueller further teaches the die being coupled to the transition medium through an adhesive (64 in Fig. 3B; Col. 9, line 65).

Regarding claims 12 and 13, Schueller, Freyman et al. and Zenner et al. teach substantially the entire claimed structure as applied to claim 1, above, wherein Schueller further teaches the metallized polymer layer/flexible dielectric tape having conventional dielectric and conductive layers (60 and 59 respectively in Fig. 3B; Col. 7) and solder balls being mounted to the second side of the metallized polymer layer and

electrically contacting the etched circuit in a conductive layer of the tape carrier (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claims 14 and 15, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claims 1, 12 and 13 above, wherein Schueller further teaches the solder balls being arranged in a grid fashion under the position for the silicon die (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6) and electrically connecting the package to a PCB (Fig. 3B; Col. 7, lines 32 and 58; Col. 5-12; Fig. 6).

Regarding claims 16 and 17, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1, above, wherein Schueller further teaches a variety of configurations (see Fig. 3A-3D, 5 and 6) where the a cross-sectional area of the die is nearly equal to or substantially less than that of the rigid transition medium (Col. 8-12) and Zenner et al. teach the die being thinned/processed/lapped to the desired first thickness (see Col. 2 and 4).

Regarding claim 18, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1, above, wherein Schueller teaches the package being a BGA package.

Regarding claim 19, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1, above, but fail to teach die having a volume being less than that of the rigid transition medium.

As explained above, Schueller teaches the thickness of the transition medium being 100-250 microns (Col. 9, line 49) and the cross-sectional area of the die being less than that of the rigid transition medium (Fig. 3A-3D; Col. 8-12).

Zenner et al. teach using a high density/thin package having the die thickness of about less than 100 microns or preferably less than 20 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the die having a volume being less than that of the rigid transition medium as taught by Zenner et al. so that the die support and the thermal performance can be improved in Freyman et al., Zenner et al. and Schueller's IC package.

Regarding claim 49, Schueller discloses an integrated circuit (IC)/Ball Grid Array (BGA) package having a single or multiple IC dice (Fig. 3B; Col. 13, line 64), the package comprising:

- an IC die (52 in Fig. 3A) having a front side, backside and a first thickness between the front and back sides, where the bonding pads (Col. 8, line 25) are formed on the front side
- a metallized polymer layer/tape substrate (58/59/60 in Fig. 3A) having a first side and a second side wherein the bonding pads are electrically coupled to the

features/patterns (59 in Fig. 3A) of the metallized polymer layer/tape using bonding wires (82A in Fig. 3A)

- a transition medium/support structure between the IC die and the metallized polymer layer (50A in Fig. 3A) having only an adhesive layer (64A in Fig. 3A) between the two where the transition medium/support structure has a second thickness, the second thickness being relatively uniform and none of the bonding pads being electrically coupled to the transition medium
- the backside of the IC die faces toward the transition medium and the front side of the IC die faces away from the metallized polymer layer/tape
- the IC die, metallized polymer layer/tape and transition medium are parallel planes, and
- solder balls (54 in Fig. 3A) below the metallized polymer layer/tape and the IC die electrically coupled to the bonding pads

(Fig. 3A; Col. 8, line 24; Col. 7, line 3- Col.1, line 12).

Schueller further teaches using a single transition medium/support structure having a second thickness/layer of 100-250 microns (Col. 9, line 49) or using a plurality of those layers (Col. 11, line 12) but fails to teach:

- a) the second thickness being greater than the first thickness, and
- b) a first and a second edge of the transition medium being coincident with those of the silicon die respectively.

a) Zenner et al. teach using a high density/thin package having a die thickness of about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total

volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

b) Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second thickness of transition medium being greater than the first thickness as taught by Zenner et al. and the first and second edge of the transition medium being coincident with those of the silicon die respectively so that the thermal stress can be reduced, the functionality/reliability of the package can be improved and processing can be simplified in Schueller's IC package.

Regarding claim 50, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49, above, wherein Schueller teaches the front side of the die being faced away from the metallized polymer layer/tape (see Fig. 3A).

Regarding claim 51, Schueller and Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49, above, wherein Schueller teaches

the IC die, metallized polymer layer/tape and transition medium being three parallel planes (see Fig. 3A).

Regarding claim 52, Schueller and Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49, above, wherein Schueller teaches the transition medium/support structure having a single/relatively uniform thickness (see Fig. 3A).

Regarding claim 53, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49, above, wherein Schueller further teaches the packages being sawed/diced into a single IC die/package (Col. 13, line 64).

Regarding claims 54 and 56, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49, above, wherein Schueller further teaches the bonding pads being electrically coupled to the features/patterns of the metallized polymer layer/tape using bonding wires (82A in Fig. 3A) and none of the bonding pads being electrically coupled to the transition medium.

Regarding claim 55, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49, above, wherein Schueller further teaches the transition medium/support comprising a single or multilayered structure including non-polymer material, ceramic or a combination of metal and non-metal/epoxy PCB material (Col. 9, line 58; Col. 10, line 27; Col. 11, line 12).

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Regarding claim 57, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49 above, wherein Schueller further teaches having only an adhesive layer (64 in Fig. 3A) between the transition medium/support structure and IC die.

Regarding claim 58, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49 above, wherein Schueller teaches the back side of the die facing toward the transition medium (see Fig. 3A).

Regarding claim 59, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49 above, wherein Schueller teaches the IC package being the BGA package (see Fig. 3A).

Regarding claim 61, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 49 above, wherein Schueller further teaches the solder balls (54 in Fig. 3A) below the metallized polymer layer/tape and the IC die being electrically coupled to the bonding pads (Col. 8, line 25).

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949), Freyman et al. (US Pat. 5985695) and Kimura (US Pat. 5663594) as applied to claim 20 above, and further in view of APA.

Regarding claim 21, Schueller, Kimura and Freyman et al. teach substantially the entire claimed structure as applied to claim 20 above, except the mold cap/encapsulant having a CTE similar to that of the transition medium.

Schueller further teaches the transition medium/support structure being made of a variety of material including a PCB/FR-4 type material (Col. 10, lines 18-28).

Such conventional substrate material as PCB/package substrate, resin/FR-4 substrate, etc. have typical CTE in a range of $12-17 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2).

Conventional encapsulant and molding material used in chip packaging and encapsulation technology art have thermal coefficient of expansion (CTE) range of $7-15 \times 10^{-6}/^{\circ}\text{C}$ (see Table 2- admitted prior art).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the mold cap/encapsulant having a similar values of the CTE to those of the transition medium as taught by Schueller and APA so that the thermal stress can be reduced in Kimura and Freyman et al. and Schueller's IC package.

6. Claims 25 and 62-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949) in view of Zenner et al (US Pat. 6246010), admitted prior art (APA) and Freyman et al. (US Pat. 5985695).

Regarding claim 25, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a metallized polymer layer (MPL)/flexible dielectric tape carrier (FDTC) substrate (59/60 in Fig. 3B/3A; Col. 7, lines 30-35) having a first/top side and a second/bottom side, the MPL/FDT defining a first thickness
- a first adhesive layers (56 in Fig. 3B) having a thickness and a CTE disposed on the tape carrier (Fig. 3B; Col. 9, line 65; Col. 8, line 12- Col. 10, line 36)
- a transition medium/support structure (50 in Fig. 3B/3A) having first and second surfaces where the first surface engages the first adhesive layer and the transition medium/support structure having a thickness and a CTE
- a second adhesive layer (64 in Fig. 3B) having a thickness and a CTE disposed on the transition medium/support structure (Fig. 3B; Col. 8, line 12- Col. 10, line 36)
- a silicon die (52 in Fig. 3B/3A) having a thickness being disposed on the second adhesive layer, and
- a conventional plastic encapsulant/mold cap encapsulating the first adhesive layer, transition medium, second adhesive layer and the die (mold cap not numerically referenced- see Fig. 3B; Col. 8, line 40), wherein the mold cap and the MPL/FDTC define a package thickness, and
- the thickness of the adhesive layers, transition medium and die is approximately half the package thickness (see Fig. 3B)

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller further teaches selecting the transition medium/support having similar CTE as that of the conventional package substrate material (Col. 8, line 53) to minimize thermal stress and further teaches the transition medium/support having a thickness/layer of 100-250 microns (Col. 9, line 49) and being made of PCB/FR-4 type material (Col. 10, line 18-27).

Schueller fails to teach:

- a) the thickness of the die being less than that of the transition medium; the thickness of the adhesive layers, transition medium and die is nearly equivalent to or same as the half of the package thickness, and a first and a second edge of the transition medium being coincident with those of the die respectively, and
- b) the transition medium and the mold cap have approximately same CTE so as to reduce the thermal stress on the die due to thermal cycling

- a) Zenner et al. teach using a high density/thin package having a die thickness of about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

Furthermore, the determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in

the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

b) APA teaches the conventional substrate material as PCB, FR-4/package substrate resin, etc. have typical CTE in the range of $12-17 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2).

APA further teaches the mold cap having a CTE of about $7-15 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2), the values within the range being approximately the same for the transition medium/support structure and the mold cap.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate elements a) and b) as taught by Zenner et al., APA and Freyman et al. so that the thermal stress on the die due to thermal cycling or temperature extremes can be reduced, processing can be simplified and the package dimensions can be improved in Schueller's IC package.

Regarding claim 62, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3B/3A) having a first thickness
- a substrate comprising a metallized polymer layer/tape (59/60 in Fig. 3B/3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3B/3A) disposed between the silicon die and the substrate, the transition medium/support structure having a second thickness, and
- a conventional plastic encapsulant/mold cap encapsulating the die and the transition medium (mold cap not numerically referenced- see Fig. 3B; Col. 8, line 40),

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Furthermore, Schueller teaches selecting the transition medium/support having similar CTE as that of the conventional package substrate material (Col. 8, line 53) to minimize thermal stress and further teaches the transition medium/support having a thickness/layer of 100-250 microns (Col. 9, line 49) and being made of PCB/FR-4 type material (Col. 10, line 18-27).

Schueller fails to teach:

a) the thickness of the transition medium being greater than that of the die and a first and a second edge of the transition medium being coincident with those of the die respectively, and

b) the transition medium and the plastic encapsulant having approximately equal CTE.

a) Zenner et al. teach using a high density/thin package having a die thickness of about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

b) APA teaches the conventional substrate material as PCB, FR-4/package substrate resin, etc. have typical CTE in the range of $12-17 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2).

APA further teaches the mold cap having a CTE of about $7-15 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2), the values within the range being approximately the same for the transition medium/support structure and the mold cap.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the thickness of the transition medium being greater than that of the die and the transition medium, the first and a second edge of the transition medium being coincident with those of the die respectively and the plastic encapsulant having approximately equal as taught by Zenner et al., Freyman et al. and APA so that

the thermal stress can be reduced and the functionality/reliability of the package can be improved in Schueller's IC package.

Regarding claim 63, Schueller, Zenner et al., Freyman et al. and APA teach substantially the entire claimed structure as applied to claim 62 above, wherein Schueller further teaches the transition medium comprising a first adhesive layer (56 in Fig. 3B) disposed between the transition medium and the substrate and a second adhesive layer (64 in Fig. 3B) disposed between the transition medium and the die (Fig. 3B; Col. 9, line 65; Col. 8, line 12- Col. 10, line 36).

Regarding claim 64, Schueller, Zenner et al., APA and Freyman et al. teach substantially the entire claimed structure as applied to claim 62 above, wherein Schueller further teaches the distance from the top of the plastic encapsulant/mold cap being the package thickness, wherein the die is positioned approximately in the middle of the package thickness (see Fig. 3B).

The determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

Regarding claim 65, Schueller, Zenner et al., APA and Freyman et al. teach substantially the entire claimed structure as applied to claim 62 above, wherein Schueller further teaches the transition medium/support structure being made of conventional nonconductive epoxy/PCB/FR-4 type material (Col. 10, line 18-27).

Regarding claim 66, Schueller, Zenner et al., Freyman et al. and APA teach substantially the entire claimed structure as applied to claim 1 above, except the range of CTE for the transition medium being between $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$.

Schueller further teaches the transition medium/support structure being made of PCB/FR-4 type material (Col. 10, line 18-27).

APA teaches the conventional material/substrates as PCB/plastic, FR-4/package substrate, etc. have typical CTE in the range of $12\text{-}17 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the transition medium having the CTE of the transition medium being between $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$ as taught by Schueller and APA so that the thermal stress can be reduced in APA, Freyman et al., Zenner et al. and Schueller's IC package.

Regarding claim 67, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3B/3A) having a first thickness

- a metallized polymer layer (MPL)/tape substrate (59/60 in Fig. 3B/3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3B/3A) disposed between the silicon die and the MPL, the transition medium/support structure having a second thickness, and
- a conventional plastic encapsulant/mold cap encapsulating the die and the transition medium (mold cap not numerically referenced- see Fig. 3B; Col. 8, line 40),

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Furthermore, Schueller teaches selecting the transition medium/support having similar CTE as that of the conventional package substrate material (Col. 8, line 53) to minimize thermal stress and further teaches the transition medium/support having a thickness/layer of 100-250 microns (Col. 9, line 49) and being made of PCB/FR-4 type material (Col. 10, line 18-27).

Schueller fails to teach:

- a) the first thickness of the die being less than the second thickness and a first and a second edge of the transition medium being coincident with those of the die respectively, and
 - b) the transition medium and the plastic encapsulant having approximately equal CTE.
- a) Zenner et al. teach using a high density/thin package having a die thickness of about less than 100 microns or preferably less than 20 microns and a package

thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

b) APA teaches the conventional substrate material as PCB, FR-4/package substrate resin, etc. have typical CTE in the range of $12-17 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2).

APA further teaches the mold cap having a CTE of about $7-15 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2), the values within the range being approximately the same for the transition medium/support structure and the mold cap.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the first thickness of the die being less than the second thickness, the first and a second edge of the transition medium being coincident with those of the die respectively and the plastic encapsulant having approximately equal as taught by Zenner et al., APA and Freyman et al. so that the thermal stress can be reduced and the functionality/reliability of the package can be improved in Schueller's IC package.

Regarding claim 68, Schueller, Zenner et al., APA and Freyman et al. teach substantially the entire claimed structure as applied to claim 67 above, except the CTE of the transition medium being greater than that of the silicon die and less than that of the plastic encapsulant.

APA further teaches the ranges of the package substrate/transition medium being $12-17 \times 10^{-6}/^{\circ}\text{C}$, the mold cap/encapsulant being $7-15 \times 10^{-6}/^{\circ}\text{C}$ and silicon die being $2.6-6.0 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2), such that one or more values from these ranges can be selected to satisfy the requirement for the transition medium having the CTE being greater than that of the silicon die and less than that of the plastic encapsulant.

Furthermore, the determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio and CTE/composition of various components in the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress reduction due to thermal mismatch.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the transition medium being greater than that of the silicon die and less than that of the plastic encapsulant as taught by Schueller and APA so that the thermal stress can be reduced and the functionality/reliability of the package can be improved in Freyman et al., Zenner et al., APA and Schueller's IC package.

Regarding claim 69, Schueller discloses an integrated circuit (IC)/BGA package comprising:

- a silicon die (52 in Fig. 3B/3A) having a first thickness
- a metallized polymer layer (MPL)/tape substrate (59/60 in Fig. 3B/3A; Col. 7, line 30) having a first/top side and a second/bottom side, and
- a transition medium/support structure (50 in Fig. 3B/3A) disposed between the silicon die and the MPL, the transition medium/support structure having a second thickness, and
- the package having external connections/solder balls (54 in Fig. 3B) and being capable of being mounted to a printed circuit board (PCB)

(Fig. 3B/3A; Col. 8, line 12- Col. 10, line 36; Col. 5, line 36- Col. 6, line 55).

Schueller further teaches selecting the transition medium/support having similar CTE as that of the conventional package substrate material (Col. 8, line 53) to minimize thermal stress and further teaches the transition medium/support having a thickness/layer of 100-250 microns (Col. 9, line 49) and being made of PCB/FR-4 type material (Col. 10, line 18-27).

Schueller fails to teach:

a) the first thickness of the die being less than the second thickness and a first and a second edge of the transition medium being coincident with those of the die respectively, and

b) the transition medium having a CTE being less than the PCB and being greater than that of the silicon die.

a) Zenner et al. teach using a high density/thin package having a die thickness of about less than 100 microns or preferably less than 20 microns and a package thickness of about 275 microns (Col. 2, line 15-22; Col. 3, line 55) to reduce the total volume of the package, thermal stress, stress related failures and to improve functionality/reliability due to the thermal expansion mismatch (Col. 4, line 55- Col. 5, line 20).

Freyman et al. teach a BGA package (Fig. 7) having dimensions of a flexible substrate, an adhesive medium/transition and a die (201, 703 and 41 respectively in Fig. 7) such that a first and a second edge of the adhesive medium/transition medium are coincident with those of the die (see 703 and 41 respectively in Fig. 7; Col. 9, lines 1-5).

b) APA further teaches the ranges of the package substrate/transition medium being $12-17 \times 10^{-6}/^{\circ}\text{C}$, the PCB being $17 \times 10^{-6}/^{\circ}\text{C}$ and silicon die being $2.6-6.0 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2), such that one or more values from these ranges can be selected to satisfy the requirement for the transition medium having the CTE being greater than that of the silicon die and less than that of the PCB.

Furthermore, the determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio and CTE/composition of various components in the chip packaging and encapsulation technology art is a

subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress reduction due to thermal mismatch.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the first thickness of the die being less than the second thickness, the first and second edge of the transition medium being coincident with those of the die respectively and the transition medium having a CTE being less than the PCB and being greater than that of the silicon die as taught by Zenner et al., Freyman et al. and APA so that the thermal stress can be reduced, the functionality/reliability of the package can be improved and processing can be simplified in Schueller's IC package.

7. Claims 3, 5, 11, 60 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller (US Pat. 5866949), Zenner et al (US Pat. 6246010) and Freyman et al. (US Pat. 5985695) as applied to claims 1, 10 and 49 above, and further in view of admitted prior art (APA).

Regarding claims 3 and 11, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claim 1 above, Schueller further discloses encapsulating the silicon die and the transition medium with a conventional plastic encapsulant/mold cap, but fail to teach the encapsulant and adhesive having a thermal coefficient of expansion (CTE) approximately in a range of $7-15 \times 10^{-6}/^{\circ}\text{C}$ and $58 \times 10^{-6}/^{\circ}\text{C}$ respectively.

Conventional encapsulant/mold cap and adhesives used in chip packaging and encapsulation technology art have thermal coefficient of expansion (CTE) range of $7\text{--}15 \times 10^{-6}/^{\circ}\text{C}$ and approximately $58 \times 10^{-6}/^{\circ}\text{C}$ respectively (Table 2- admitted prior art).

Furthermore, the determination of parameters such as a thickness of a substrate/metallized polymer, plastic encapsulant/mold, finished package including the die, substrate and the encapsulant, thickness/area/volume ratio of various components, relative position and an arrangement of various components within the package, etc. in the chip packaging and encapsulation technology art is a subject of routine experimentation and optimization to achieve the desired thermal, dimensional/mechanical and electrical/reliability requirements including weight/size, rigidity/strength and stress distribution.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plastic encapsulant and adhesive having approximate CTE range of $7\text{--}15 \times 10^{-6}/^{\circ}\text{C}$ and $58 \times 10^{-6}/^{\circ}\text{C}$ respectively as taught by APA so that the thermal stress can be reduced in Freyman et al., Zenner et al. and Schueller's package.

Regarding claims 5, 60 and 70, Schueller, Zenner et al. and Freyman et al. teach substantially the entire claimed structure as applied to claims 1, 3 and 49 above, except the range of CTE for the transition medium being between $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$ or the CTE of the transition medium and the plastic encapsulant being approximately equal respectively.

Schueller further teaches the transition medium/support structure being made of PCB/FR-4 type material (Col. 10, line 18-27).

APA teaches the conventional substrate material such as a PCB/package substrate, FR-4/resin substrate, etc. having typical CTE in the range of $12-17 \times 10^{-6}/^{\circ}\text{C}$ and the encapsulant/mold cap having the CTE range of $7-15 \times 10^{-6}/^{\circ}\text{C}$ (see admitted prior art-Table 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the transition medium having the CTE of the transition medium being between $7 \times 10^{-6}/^{\circ}\text{C}$ and $17 \times 10^{-6}/^{\circ}\text{C}$ or the CTE of the transition medium and the plastic encapsulant being approximately equal as taught by Schueller and APA so that the thermal stress can be reduced in Freyman et al., Zenner et al. and Schueller's IC package.

Response to Arguments

8. Applicant's arguments with respect to claims 1-25 and 49-70 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Art Unit: 2811

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

05-20-04


NITIN PAREKH

PATENT EXAMINER

TECHNOLOGY CENTER 2800